ABSTRACT OF THE DISCLOSURE

A semiconductor device is provided which is capable of avoiding malfunction and latchup breakdown resulting from negative variation of high-voltage-side floating offset voltage (VS). In the upper surface of an n-type impurity region (28), a p^+-type impurity region (33) is formed between an NMOS (14) and a PMOS (15) and in contact with a p-type well (29). An electrode (41) resides on the p^+-type impurity region (33) and the electrode (41) is connected to a high-voltage-side floating offset voltage (VS). The p^+-type impurity region (33) has a higher impurity concentration than the p-type well (29) and is shallower than the p-type well (29). Between the p^+-type impurity region (33) and the PMOS (15), an n^+-type impurity region (32) is formed in the upper surface of the n-type impurity region (28). An electrode (40) resides on the n^+-type impurity region (32) and the electrode (40) is connected to a high-voltage-side floating supply absolute voltage (VB).